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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,534	10/06/2003	Anthony Yap Wong	PS-105	2533

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STUART T AUVINEN
429 26TH AVENUE
SANTA CRUZ, CA 95062-5319

EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,534	WONG, ANTHONY YAP	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *2-6 and 14-16* is/are withdrawn from consideration.

5)☒ Claim(s) *17-20* is/are allowed.

6)☒ Claim(s) *7-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is responsive to the amendment filed on 1/21/05.

2. The objections to the specification and the drawings, and the rejection under 35 U.S.C. 112, 2nd paragraph in the last office action have been overcome based on applicant's amendment.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Talaga, Jr. (USP 5,942,921) in view of Kuo (USP 6,661,713).

With respect to claim 1, Talaga, Jr. discloses in Figure 3 a circuit, which includes: a source-input node (gate of 306) having a source-input voltage (VIN) that is varied by a voltage source (i.e., the source that is used to generated VIN), the circuit in Figure 3 sensing the source-input voltage of the source-input node; a voltage node (node receiving voltage +VCC) having a voltage (+VCC); a first current source (306) responsive to the source-input voltage (VIN) for generating a first current (current of 306); a first resistor (308) coupled tot the first current source (306) for generating a compared-input voltage (voltage at the junction node of 306 and 308 which is input to the (-) terminal of 202) in response to the first current and varying with variations in the first current; a second current source (302) for generating a second current (current of 302) that is insensitive to variations in the source-input voltage (because 302 does not

responsive to VIN); a second resistor (304) coupled to the second current source for generating a reference voltage (voltage at the junction node of 302 and 304 which is input to the (+) terminal of 202); and a comparator (202) for comparing the compare-input voltage to the reference voltage (i.e., comparing voltages at the (-) and the (+) terminals of the comparator 202) and generating an output voltage (VOUT) indicates when the compare-input voltage is above the reference voltage (i.e., based on the logic value of VOUT). The Talaga, Jr. reference does not discloses that the voltage +VCC is a stable voltage that is insensitive to variations/changes in a supply voltage. However, the Kuo reference discloses a band-gap circuit (Figure 2) that provides a stable voltage and is insensitive to temperature, process and power supply voltage variations (Col. 2, lines 18-22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit in Figure 3 of the Talaga, Jr. reference by using specific band-gap circuit (Figure 2 of Kuo) for generating/providing the voltage +VCC in Figure 2 of the Talaga, Jr. reference for the purpose of improving the performance of the circuitry such as the comparison result is more accuracy because the voltage generated by the Kuo reference is stable and is insensitive to power supply voltage, temperature and process variations. Thus, this modification/combination meets all the limitations of claim 1.

Response to Arguments

5. Applicant's arguments filed 1/21/05 have been fully considered but they are not persuasive.

Applicant argues that the combination of Talaga, Jr. and Kuo does not meet the limitations of claim 1 because Talaga's Figure 3 +VCC teaches away from claim 1 which recites a stable voltage that is relative to changes in a supply voltage. However, this argument is not

persuasive because the voltage +VCC in Figure 3 of Talaga, Jr. must be provided from a voltage generator and it is desired that the voltage that is generated to be as stable as possible, so the use of a band-gap circuit (Figure 2 of Kuo) for generating/providing the voltage +VCC in Figure 3 of the Talaga, Jr. reference will improving the performance of the circuitry such as the comparison result is more accuracy because the voltage generated by the Kuo reference is stable and is insensitive to power supply voltage, temperature and process variations.

Allowable Subject Matter

6. Claims 7-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 7 would be allowed because the prior art of record fails to disclose or suggest the first current source including a first mirror transistor, a first setting transistor and a first sensing transistor; and wherein the second current source including a second mirror transistor, a second setting transistor and a second sensing transistor with the recited connections and operations set forth therein.

Claims 8-13 would be allowed because they depend on claim 7.

7. Claims 17-20 are allowed.

Claim 17 is allowed because the prior art of record fails to disclose or suggest a circuit including, in combination with other elements, first mirror transistor means, first current-source transistor means, first sensing transistor means, second mirror transistor means, second current-source transistor means, and second sensing transistor means with the recited connections and operations set forth therein.

Claims 18-20 are allowed because they depend on claim 17.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 8, 2005

Long Nguyen
Primary Examiner
Art Unit: 2816